Large Area >8 kV SiC GTO Thyristors with innovative Anode-Gate designs

Siddarth G. Sundaresan, Hany Issa, Deepak Veereddy and Ranbir Singh

GeneSiC Semiconductor, Inc., 43670 Trade Center Pl, Suite 155, Dulles, VA 20166, USA

sid@genesicsemi.com

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Abstract. This study is focused on the design and fabrication of large-area (4.1x4.1 mm^2 and 8.2x8.2 mm^2), 8.1 kV 4H-SiC GTO Thyristors. The anode and gate fingers of Thyristors were designed with involute, cellular or hexagonal patterns. Forward blocking voltages as high as 8106 V and On-state voltage drop (Von) and differential specific on-resistance ($R_{on,sp}$) as low as 3.8 V and 6 mΩ-cm^2 at 100 A/cm^2 were measured on these devices. About 59% of 4.1 x4.1 mm^2 and 29% of 8.2x8.2 mm^2 Thyristors blocked voltages in excess of 6 kV. Detailed investigations revealed the impact of different anode/gate finger geometries on the device characteristics. Preliminary pulsed power characterization of the GTO Thyristors was also performed.

Introduction

There is a strong interest for the development of a high voltage, high current, high frequency Silicon Carbide (SiC) based switches for utility applications. These applications demand high frequency power conversion with an order of magnitude higher power levels at an order of magnitude higher frequency as compared to what is achievable with contemporary silicon power devices. As compared to unipolar devices like JFETs and MOSFETs, bipolar-mode switches like Gate Turn-Off (GTO) Thyristors offer low conduction losses in >6 kV ratings, due to high level of minority carrier injection into the low doped voltage blocking region [1-3]. This paper focuses on large area (4.1x4.1 mm^2 and 8.2x8.2 mm^2) > 8 kV SiC GTO Thyristors recently designed and fabricated at GeneSiC.

Epilayer and Device Design

Epilayer Design The first step in the (N^+P-NP^+) Thyristor epilayer design was to determine the doping and thickness of the voltage blocking p^- layer. Direct integration of the ionization integral was performed to simulate the breakdown voltages for different epilayer thickness/doping combinations. The ideal unipolar parallel plane breakdown voltage for an epilayer thickness of 60 µm was simulated to be 9700 V. The other layers were subsequently designed for optimizing the GTO Thyristor device characteristics.

Device Design/Layout The anode/gate fingers of the GTO Thyristors were inter-digitated in cellular, involute or hexagonal patterns (see Fig. 1) to determine their effect on on-state and turn-off capability. For each layout geometry, the anode and gate finger widths were also varied to examine their impact on the device performance. In this study, GTO Thyristors with an active area of 4.1x4.1 mm^2 and 8.2x8.2 mm^2 were used. A summary of the different Gate/Anode designs investigated in this study is given in Table 1. A combination of mesa and junction termination extension (JTE) based edge termination strategies were employed for optimizing the forward blocking characteristics.

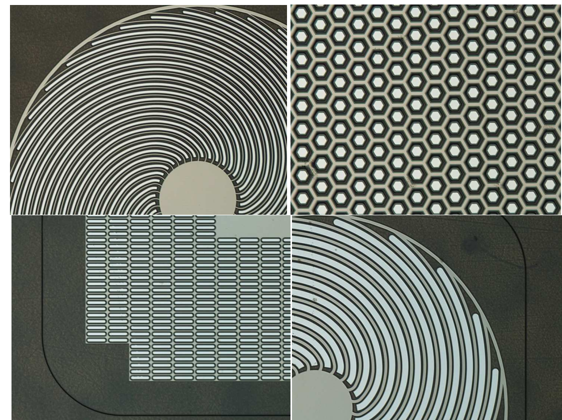

Figure 1: Anode/Gate designs of SiC GTO thyristors fabricated on the same wafer – A fine Involute, Hex, Coarse Involute and raster.

Table 1: Summary of various anode-gate variations investigated in the first batch of GeneSiC's GTO

Device ID	Pattern	Anode width (µm)	Gate width (µm)
I-24-21	Involute	24	21
I-48-21	Involute	48	21
I-48-34	Involute	48	34
I-117-21	Involute	117	21
C-24-15	Cellular	24	15
C-24-24	Cellular	24	24
C-42-15	Cellular	42	15
H-24-21	Hexagonal	24	21

Device Fabrication

Reactive ion etching (RIE) of the SiC was performed for isolating the individual devices, and for providing gate access trenches for connecting the gate fingers. The channel-stop, gate and JTE implantations were then performed by using various masking techniques. High-temperature annealing at 1690 °C was performed to heal the implant-induced lattice damage and to electrically activate the implanted dopants. Next, ohmic contacts to the anode and gate fingers were formed by metal deposition followed by rapid thermal annealing. A thick overlayer metal was then patterned on top of the ohmic contacts to decrease the lateral resistance along the gate fingers. A two-level metallization process incorporating a novel planarization/ gap-fill scheme was developed and implemented to connect the anode and gate fingers of the GTO Thyristors. A cross-sectional SEM image, depicting the two-level metallization scheme is shown in Fig. 2.

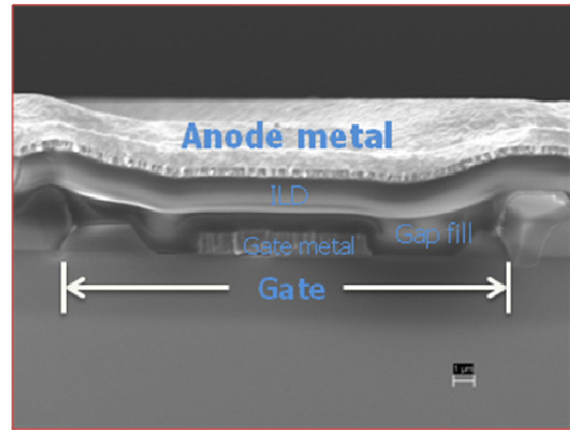

Figure 2: Cross-sectional SEM image depicting the two-level metallization scheme incorporating a novel planarization/gap-fill process

Device Characterization

On-state and blocking characteristics An automated test system was used to investigate the on-state and forward blocking characteristics of the Thyristors. The devices were turned on by increasing the gate current in 10 mA steps until the device latched on, while keeping the V_{AK} bias fixed at 5 V. Representative forward I-V curves measured on a 4.1x 4.1 mm^2 GTO thyristor are shown in Figure 3.

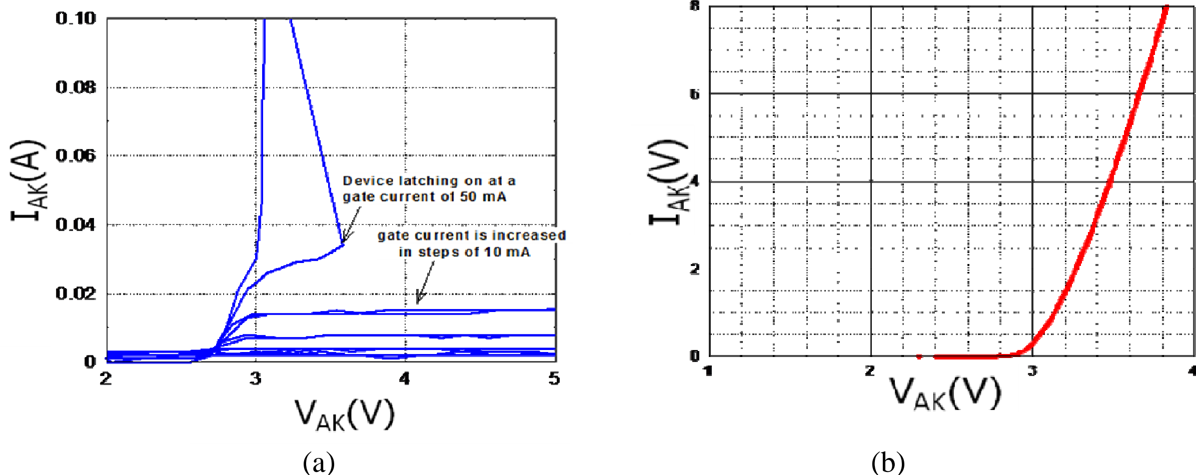

Figure 3: Turn-on I-V characteristics measured on a representative 4.1 x 4.1 mm^2 GTO Thyristor at (a) low currents and (b) high currents

A very low V_{on} of 3.8 V and a differential specific on-resistance of 6 mΩ-cm^2 at 100 A/cm^2 was measured on the 4.1x 4.1 mm^2 Thyristors (normalized to an active area of 7.3 mm^2), indicating a high-level of conductivity modulation of the p- drift region and the achievement of low contact resistances, especially for the p+ anode contacts. Some devices were found to block voltages in excess of 8.1 kV (an example curve is shown in Figure 4(a)). This represents > 84% of the theoretical (unipolar) breakdown voltage of 9700 V for the p- epilayer used for fabrication. This result was made possible by the optimized edge termination and surface passivation schemes utilized for fabricating these Thyristors. A histogram of forward blocking voltages measured on all devices from a 3 inch wafer is shown in Figure 4(b). It was found that 29% of all 8.1x8.1 mm^2 devices and 59% of all 4.1x4.1 mm^2 devices blocked voltages in excess of 6 kV.

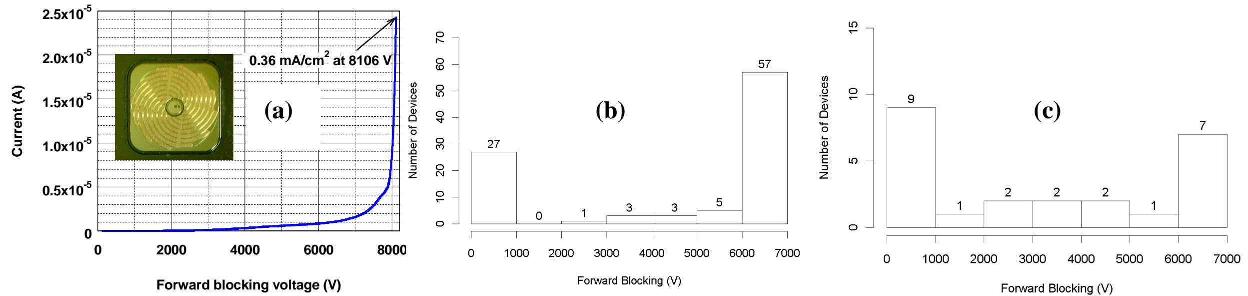

Figure 4(a) Forward blocking voltage measured on a representative 4.1x4.1 mm^2 involute GTO Thyristor (b) Histogram of forward blocking voltages measured on (b) 4.1x 4.1 mm^2 devices and (c) 8.2 x 8.2 mm^2 devices from a 3" SiC wafer.

Infuence of gate/anode geometry on device characteristics

Influence of Anode widths (Involute) Devices I-117-21 and I-24-21 (see Table 1) were compared from 3 wafers fabricated in this study to examine the influence of the Anode finger widths on the on-state characteristics. These devices had gate fingers of equal width (21 μm). It can be seen from Fig. 5 that the Gate currents required for triggering the Thyristors decreased for devices with wider Anodes. An examination of the I-117-21, I-48-21 and I-24-21 device layouts show that the current impressed on the central Gate pad gets divided among 12, 24 and 36 (equally wide) gate fingers, respectively. Thus, the effective gate current per finger is lower for the devices with wider Anodes, and this translates to a higher gate trigger current for these devices.

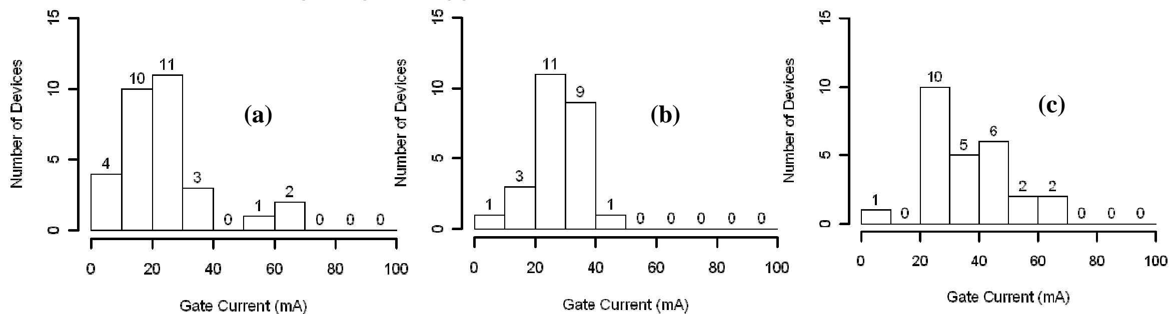

Figure 5: Gate trigger currents required for turning on (a) 117 μm wide, (b) 48 μm wide and (c) 24 μm wide involute GTO Thyristors. The data represents devices from 3 wafers. Note that all these devices have a constant gate width of 21 μm.

However, similarly low V_{on} and differential specific on-resistances in the range of 6-7 mΩ-cm^2 were measured on the Thyristors with different Anode widths shown in Fig. 5. This indicates (a) optmized ohmic contacts to the p+ Anode layers and (b) the difference in Anode widths does not significantly affect their minority carrier injection efficiencies. However, the similar V_{on}'s could also be a reflection of the relatively low currents (10 A) at which the measurements were performed, and higher current measurements may reveal discrepancies.

Influence of gate widths Devices with equal anode widths (48 µm) but different (20 µm and 36 µm) gate widths were also compared to examine the impact of gate width on the on-state Thyristor characteristics. It was found that that about 56 devices (from 3 wafers) had no Anode-Gate shorting as compared to only 27 devices with a narrower gate. There was no discernable difference in the gate trigger currents between the devices with wide and narrow gates, which means that there is no significant voltage drop along the gate fingers, even for the narrower gate devices. The increased Anode-Gate shorting on the narrower gate devices could be attributed to too tight lithographic tolerances.

Cellular and Hexagonal Thyristors It was also found that the devices with cellular and hexagonal geometry suffered from a large density of Anode-Gate shorting, and this precluded us form making any useful comparisons of their device characteristics with the involute Thyristors.

Device Packaging and Pulsed Power Performance

A custom designed package was used for packaging the GTO Thyristors. Some of the packaged GTO Thyristor dies were investigated for possible use in pulsed power applications. The Anode-Cathode bias was charged to 1-4 kV using a 500 nF capacitor and the devices were triggered by applying a gate circuit with a 1.4A capability. The time evolution of switching currents for two different charging voltages impressed upon a 4.1x4.1 mm^2 involute Thyristor is shown in Fig. 6. It can be seen that a maximum current of 600 A, with a rise time of 700 ns, was successfully switched by the device for a charging voltage of 3400 V. It can also be seen from Fig. 6 that increasing the charging voltage increases the pulsed current capability and decreases the rise time of the switch current. The switch current rise time is partly limited by the rise time of the gate current, due to the capacitances in the gate drive circuit. Further investigations are underway to correlate the influence of device geometry on pulsed power performance.

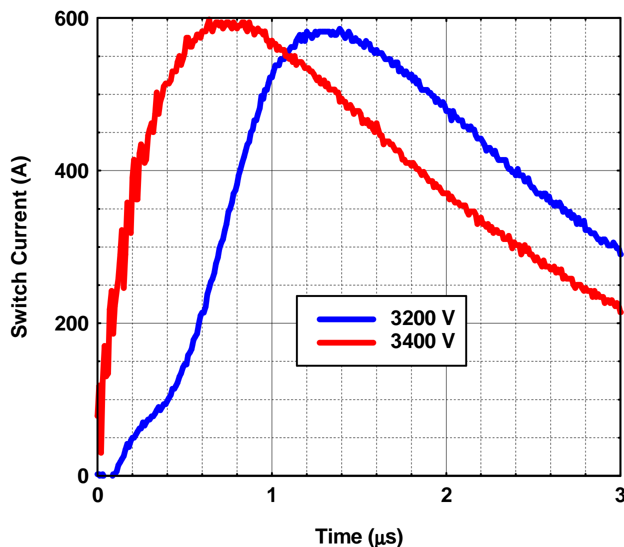

Figure 6: Evolution of switching current versus time for a 4.1x4.1 mm^2 GTO Thyristor for different charging voltages

Summary

In this study, large-area 4.1x4.1 mm^2 and 8.2x8.2 mm^2, >8 kV SiC GTO Thyristors were fabricated with optimal on-state and forward blocking characteristics. Several anode-gate inter-digitation schemes were explored and their impact on the device characteristics was discussed. The GTO Thyristors fabricated in this work were distinguished by their low $R_{on,sp}$ = 6 mΩ-cm^2 (normalized to the active area), 84% of theoretical breakdown voltage (8106 V), and low gate trigger currents. Preliminary pulsed characteristics of the Thyristors were also presented.

Acknowledgement

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