Abstract — Through a systematic study, Silicon Carbide Gate Turn Off (GTO) Thyristors with record performance are demonstrated. Several Anode-Gate interdigital schemes (raster, hex and involute) were explored to investigate their effect on the static as well as switching characteristics. An optimized edge-termination was employed that resulted in the achievement of near-theoretical forward blocking voltages (>8.1kV), and high yields (>60% on 8mmx8mm) on GTO Thyristors with 60µm/5x10^{14} cm^{-3} voltage-blocking epitaxial layers. A low differential specific on-resistance of 2.55 mΩ-cm², and low on-state voltage drop were measured at 500 A/cm². High Temperature forward I-V and reverse I-V characteristics show extremely stable performance with temperature, in contrast to state-of-the-art Si GTO Thyristors. Turn-on transient characteristics show a stable delay time of about 400 nano-seconds, and a rise-time that decreases with increasing temperature. Detailed high temperature turn-off measurements conducted using Anode-Switched mode was used to extract the value of minority carrier lifetimes as a function of temperature for the first time.

Introduction

There is a strong interest for the development of a high temperature, ultra-high power Silicon Carbide (SiC) based Thyristors for various high temperature and pulsed power applications. Modern Grid power electronics and Directed Energy Weapon systems require an order of magnitude higher power levels at an order of magnitude higher frequency as compared to what is achievable with contemporary Silicon power devices. As compared to unipolar devices like JFETs and MOSFETs, bipolar-mode switches like Gate Turn-Off Thyristors (GTO) offer low conduction losses in >6 kV ratings, due to high level of minority carrier injection into the low doped voltage blocking region. This paper focuses on large area (4x4 mm and 8x8 mm) > 8 kV SiC GTO Thyristors developed by GeneSiC. This is part of development towards >1 MW, 20 kHz power conversion systems funded by US Dept. of Energy under the Energy Storage program.

SiC GTO Thyristor Device Design

Epitaxial layer Design
The first step in the (N⁺P-NP⁺) epilayer design was to determine the doping and thickness of the voltage blocking p⁺ layer. Direct integration of the ionization integral was performed to simulate the breakdown voltages for different epilayer thickness/doping combinations, as shown in Figure 1. Ideal unipolar parallel plane breakdown voltage for an epilayer thickness of 60 µm was simulated to be 9700 V. The other layers were subsequently designed for optimizing the GTO Thyristor device characteristics.
Figure 1: Ab-initio 1D calculations of the ionization integral show that 60µm epitaxial layers show a 9700V blocking voltage capability for a unipolar device.

Device Design/Layout

The Anode/Gate fingers of the GTO Thyristors were inter-digitated in cellular, involute or hexagonal patterns (see Figure 2) to determine their effect on on-state and turn-off capability. For each layout geometry, the Anode and Gate finger widths were also varied to examine their impact on the device performance. In this study, GTO Thyristors with an active area of 4.1x4.1 mm and 8.2x8.2 mm were used. A combination of mesa and junction termination extension (JTE) based edge termination strategies were employed for optimizing the forward blocking characteristics.

Device Fabrication

Reactive ion etching (RIE) of the SiC was performed for isolating the individual devices, and for providing Gate access trenches for connecting the Gate fingers. The channel-stop, Gate and JTE implantations were then performed by using various masking techniques. High-temperature annealing at 1690 °C was performed to heal the implant-induced lattice damage and to electrically activate the implanted dopants. Next, ohmic contacts to the Anode and Gate fingers were formed by metal deposition followed by rapid thermal annealing. A thick overlayer metal was then patterned on top of the ohmic contacts to decrease the lateral resistance along the Gate fingers. A two-level metallization process incorporating a novel planarization/ gap-fill scheme was developed and implemented to connect the Anode and Gate fingers of the GTO Thyristors.
Device Characterization

On-state and blocking characteristics

An automated test system was used to investigate the on-state and forward blocking characteristics of the Thyristors. The devices were turned on by increasing the Gate current in 10 mA steps until the device latched on, while keeping the $V_{AK}$ bias fixed at 5 V. A very low $V_{on}$ of 3.8 V and a differential specific on-resistance of 6 mΩ-cm$^2$ at 100 A/cm$^2$ was measured on the 4.1x 4.1 mm Thyristors, indicating a high-level of conductivity modulation of the p-drift region and the achievement of low contact resistances, especially for the p+ Anode contacts. Some devices were found to block voltages in excess of 8.1 kV (an example curve is shown in Figure 5(a)). This represents > 84% of the theoretical (unipolar) breakdown voltage of 9700 V for the p- epilayer used for fabrication. This result was made possible by the optimized edge termination and passivation schemes utilized for fabricating these Thyristors. A histogram of forward blocking voltages measured on all devices from a 3 inch wafer is shown in Figure 5(b). It was found that 29% of all 8.1x8.1 mm devices and 59% of all 4.1x4.1 mm devices blocked voltages in excess of 6 kV.
After packaging the Thyristors, high-current (up to 50 A) measurements were performed at various temperatures. Forward I-V measurements performed at different temperatures on a 4.1 x 4.1 mm packaged Thyristor are shown in Figure 6.

The on-state measurements were performed by ramping the Anode-Cathode bias and the triggering the device into its on-state by the application of Gate current. The built-in voltage decreases slightly with increasing temperature, whereas the on-resistance shows a gradual increase with temperature. A plot of the extracted differential on-resistance as a function of temperature is shown in Figure 7. The on-resistances measured on the Thyristor are as low as 2.5 mΩ·cm². Such low values of on-resistance are an indication of the optimized SiC epilayers and device processing used for fabricating these Thyristors. Moreover the on-resistance shows a positive co-efficient of resistance, which is desirable for allows for stable parallel operation for pulsed power applications, which typically operate at 10 – 20 kA/cm².

**Turn-on characteristics**

Using low inductance packages for dynamic measurements, several tests were performed to investigate the effect of Gate current and...
Figure 8: Turn-on times measured on a 8 kV Thyristor at different Gate currents.

Figure 9: Extracted delay and rise time components of the total turn-on time measured at different Gate currents at room temperature.

In fact, it can be seen from Figure 10 that the significant portion of the decrease in rise time occurs when the temperature is increased from 25 C to 100 C. This is because the p+ ionization is calculated to increase from ~ 2% at 25 C to about 90 % at 100 C, which results in a significant increase in the current gain of the upper NPN transistor. This translates to a much faster rise time component of the total turn-on time. The delay time, i.e. the time required to build up charge in the p- and n bases is unaffected by the increase in operation temperature. A rise time of 48 ns is measured at a temperature of 200 C.
Turn-off characteristics

For performing the Gate turn-off of GTO Thyristors, the Thyristor was first switched on by applying An Anode-Cathode bias of 200 V. Then the Anode-Gate junction was reverse biased by applying a Gate voltage of 15 V and the decay in the Anode current was recorded. The hard turn-off measurements were performed at different temperatures and are summarized in Figure 11.

![Figure 11: Hard turn-off measurements performed on a packaged 8 kV SiC Thyristor fabricated at GeneSiC. An Anode current of 5.5 A is turned off at different temperatures.](image)

It can be observed in Figure 11 that the turn-off characteristics exhibit an initial steep decrease in Anode current followed by a more gradual decline. It can be noticed that the turn-off time decreases from 1.25 µs at room temperature to 2.2 µs at 200 °C. An estimation of the high-level minority carrier lifetime can be obtained from the slope of the linear portion of the characteristics shown in Figure 11. The extracted carrier lifetime is plotted as a function of temperature in Figure 12.

![Figure 12: Extracted (high-level) minority carrier lifetime from the hard turn-off measurements.](image)

It can be seen from Figure 12 that the minority carrier lifetime in the p- base increases from 1.52 µs at 25 °C to 3.8 µs at 200 °C. This increase in the minority carrier lifetime in combination with the improved emitter injection at higher temperatures is responsible for the longer turn-off times observed at higher temperatures.

Conclusions

In this study, large-area 4.1x4.1 mm and 8.2x8.2 mm, >8 kV SiC GTO Thyristors were fabricated with optimal on-state and forward blocking characteristics. Detailed high temperature switching measurements were conducted for the first time, and important materials-level parameters were determined. Differential on-resistance at ~500A/cm² was found to increase from 2.5 mΩ-cm² to 2.91 mΩ-cm² between room temperature and 200 C. Turn-on delay time was decreased from 400 nano-seconds to 50 nanoseconds as the Gate current was increased from 180mA to 2.4A. Turn-On rise time was decreased from 240 nano-seconds to 114 nano-seconds for a similar increase in Gate current. Current rise time was decreased from 114 nano-seconds at room temperature to 48 nano-seconds as the temperature was increased from room temperature to 200 C. Most of this increase occurred between room temperature and 100 C due to an increase in p-type acceptor
activation. Hard turn-off measurements conducted on GTO Thyristors show a complete turn-off of current within 1.25 μsec. This turn-off time increased to 2.2 μsec, as the temperature was increased to 200 C. An increase in turn-off time is attributed to the increase in high-level carrier lifetime in the p-base region from 1.52 μsec to 3.8 μsec between room temperature and 200 C. Many of these measurements are conducted for the first time on >6kV SiC GTO Thyristors.

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