

Rapidly Maturing SiC Junction Transistors Featuring Current Gain (β) > 130, Blocking Voltages Up To 2700 V and Stable Long-Term Operation

S.G. Sundaresan, S. Jeliaskov, B. Grummel, R. Singh

GeneSiC Semiconductor, Inc. 43670 Trade Center Pl, Suite 155, Dulles, VA 20166, USA

Email: siddarth.sundaresan@genesicsemi.com (corresponding author)

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Abstract. SiC *n*pn Junction Transistors (SJTs) with current gains as high as 132, low on-resistance of $4 \text{ m}\Omega\text{-cm}^2$, and minimal emitter-size effect are demonstrated with blocking voltages > 600 V. 2400 V-class SJTs feature blocking voltages as high as 2700 V combined with on-resistance as low as $5.5 \text{ m}\Omega\text{-cm}^2$. A significant improvement in the current gain stability under long-term high current stress is achieved for the SJTs fabricated by the high gain process.

Introduction

The static, switching and reliability characteristics of first-generation (Gen-I) 1200 V SiC SJTs were reported in [1], while 10 kV SJT results were presented in [2]. The Gen-I SiC SJTs featured a current gain (β) in the range of 70-80, robust avalanche mode operation, and < 25 ns switching capability. Subsequent refinements to the SJT design/process suite have resulted in large-area (chip size = $1.9\text{-}6.3 \text{ mm}^2$) Gen-II transistors with $\beta > 130$. The electrical characteristics of these high-gain, Gen-II SiC SJTs, 2400 V-class SiC SJTs, optimized gate drive techniques and device stability results from long-term, high-current operation are presented in this paper. The SJTs featured in this article were packaged in either plastic TO-247 or metal TO-257 headers for high temperature/switching investigations.

High-Current Gain (Gen-II) SiC SJTs

Purely majority-carrier like output characteristics with near- ∞ Early voltage are observed in the room-temperature output characteristics (see Fig. 1a) of a 3.5 mm^2 Gen-II SiC SJT, packaged in a high-temperature TO-257 header. The β in the active region is as high as 132 for drain current in the range of 6.5 A – 10 A, which corresponds to current densities of $260\text{-}400 \text{ A/cm}^2$, respectively. The current gain shows an expected negative temperature co-efficient (Fig. 1b) due to the increasing ionization of Al acceptors in the base layer. However, a β as high as 84 is observed at 250°C , which is 1.7 x higher than the current gain measured on Gen-I SJTs.

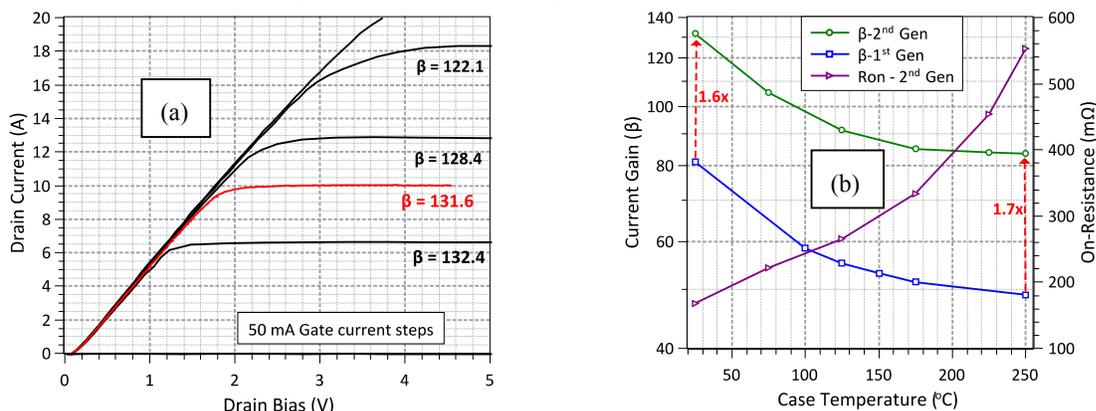


Figure 1 (a): Output characteristics of a 3.5 mm^2 SiC SJT (active area = 2.5 mm^2) fabricated by the high-gain process and (b): Temperature variation of β and Ron for 3.5 mm^2 Gen-I and Gen-II SiC SJTs.

While current gains as high as 257 were reported [3] on single-finger test BJTs, the devices reported in this paper show the highest current gain ever recorded on a multi-ampere power transistor, which also display robust blocking voltages > 600 V. The variation of β at extremely high drain current densities (up to 2000 A/cm²) was investigated by single 3 μ s-wide, 10 Hz pulsed current measurements on 3.5 mm² Gen-II SJTs (Fig. 2) to minimize any device self-heating. The current gain is relatively flat up to 800 A/cm² at all temperatures, indicating a low surface recombination velocity. The knee-current above which the β rolls off steeply reduces from 1700 A/cm² at 25°C to about 800 A/cm² at 175°C , from which the safe-operating area for high pulsed current SJT operation can be inferred. The electron mobility decreases with increasing temperature, which in turn increases the voltage drop across the low doped n- drift layer for a fixed drain current. This increased voltage drop causes the p-base/n- layer to become forward biased at a lower drain current at high temperatures, thereby lowering the knee current for β roll-off.

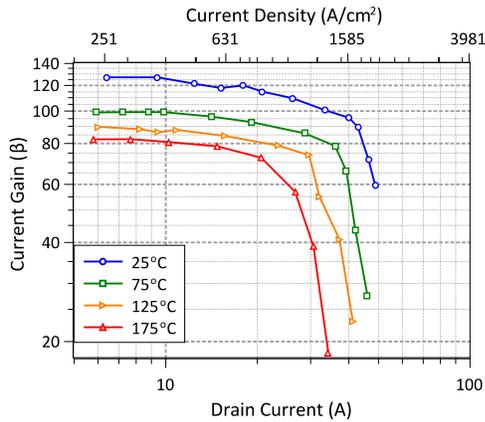


Figure 2: Current gain of a packaged 3.5 mm² SiC SJT at ultra-high current densities investigated by pulsed current measurements at various temperatures. Note that these knee currents are significantly lower than the threshold current for the onset of the Kirk effect, which is calculated as 14.3 kA/cm² using the SiC material and SJT epitaxial parameters

The β vs I_D relationship in the sub-threshold regime (Fig. 3) was investigated by Gummel-plot measurements for several test SJTs fabricated with different Source finger widths in the range of 10 - 40 μ m, by the Gen-I and Gen-II processes. In addition to the higher β values, the Gen-II process results in a drastic reduction of the emitter-size effect, which implies a significant reduction of the surface recombination velocity for the devices fabricated by the Gen-II process.

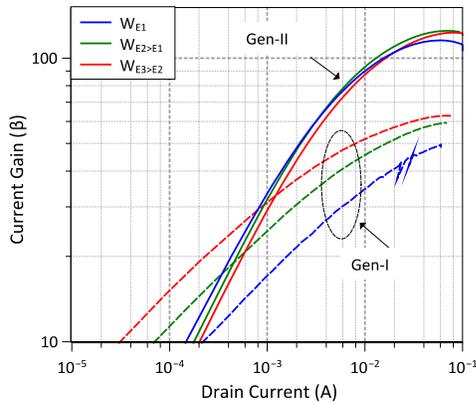


Figure 3: Emitter-size effect for SiC SJTs investigated by Gummel-plot measurements in the sub-threshold regime ($V_{DS} = 5$ V). The Gen-II SJTs demonstrate a significantly reduced emitter-size effect in addition to achieving higher values of current gain over their Gen-I counterparts.

2400 V Class SiC SJTs

The 2400 V-class SiC SJTs were fabricated on 15 μ m thick/ 8×10^{15} cm⁻³ doped SiC epilayers. These devices were fabricated using the “Gen-I” process, yielding current gains (β) in the range of 60 - 70 . Open-base breakdown I-V characteristics from over 700 , 3.5 mm² SiC SJTs fabricated on one SiC wafer are shown in Fig. 4a. A tight grouping of devices with sharp avalanche breakdown characteristics is observed in the range of 2200 – 2700 V, which corresponds to almost 100% of the avalanche rating, calculated by integrating the 4H-SiC impact ionization co-efficients. On-resistance histograms from 650 , packaged 3.5 mm² SiC SJTs with a minimum blocking voltage of 2200 V (see Fig. 4b) show values in the range of 5 – 6.5 m Ω -cm². A unipolar figure of merit

$(V_B^2/R_{ON,SP})$ in the range of 0.8 – 1.3 GW/cm² is calculated from these results, which is among the highest ever reported on a majority carrier power device (or a device without conductivity modulation of the drift layer).

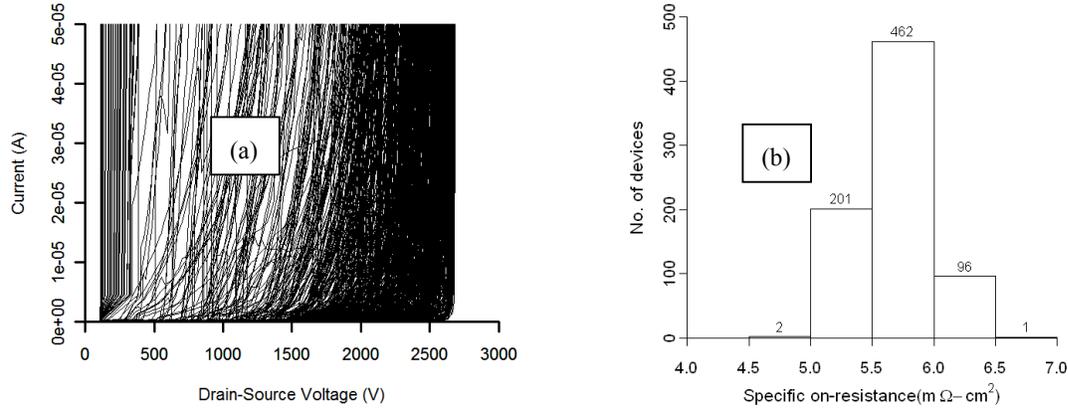


Figure 4 (a): Open-base breakdown characteristics measured on all 3.5 mm² SiC SGTs fabricated on one 100 mm SiC wafer and (b): Histogram of specific on-resistance extracted from pulsed I-V measurements on about 650 TO-247 packaged SGTs, also displaying a minimum blocking voltage of 2200 V.

A two voltage level driver schematic initially proposed in [4] (see Fig. 5a) features a lower voltage branch (V_{OL}) connected in series with an external gate resistor to maintain low steady-state driver losses, while the other gate drive IC in series with an external gate capacitor (C_{GP}) supplies a higher output voltage (V_{OH}) for achieving high dynamic gate currents. Since the Gate-Source junction of the SGT turns-on at ≈ 3 V, it can be effectively driven by gate voltages as low as 4-5 V, in stark contrast to SiC MOSFETs, which require drive voltages as high as 20 V. The values of the gate resistor and capacitor need to be optimized for minimizing the driver loss as well as the SGT switching losses. For example, at $C_{GP} = 9$ nF, the SGT drain current switching times, t_r , t_f and device switching energy losses, E_{tot} for a 1200 V/6 A SGT (see Fig. 5b) are at their combined lowest values.

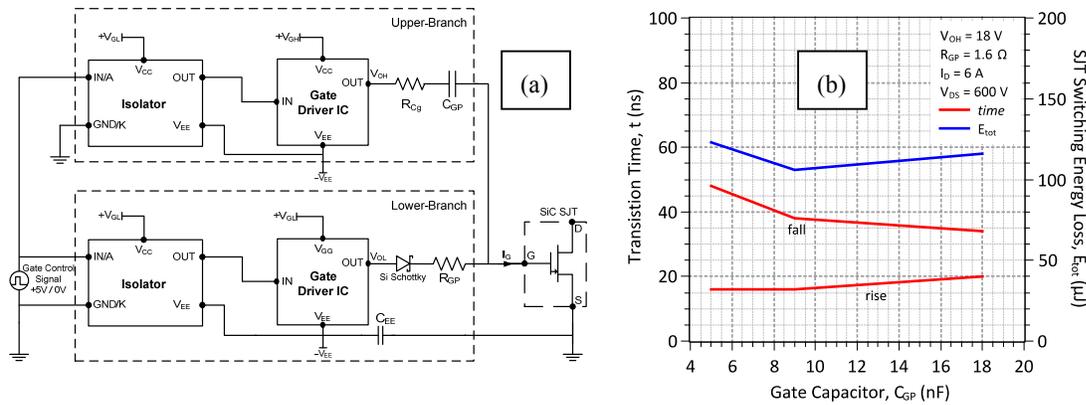


Figure 5 (a): Simplified circuit schematic of the two-voltage level gate driver developed for driving SiC SGTs (b): Effect of external gate capacitance in the two-level driver on a 1200 V/6 A SGT current turn-on and turn-off times and total device energy loss.

Temperature-independent, low Drain current rise and fall times of 10 ns and 40 ns, respectively, are observed in Fig. 6 during double pulse, inductive-load switching of a 2400 V-class 3.5 mm² SGT at 1100 V and 8 A with a two-voltage level driver. The temperature invariant switching transients confirm minimal conductivity modulation of the n- drift layer, and validate the choice of the unipolar figure of merit used to benchmark the SiC SGTs.

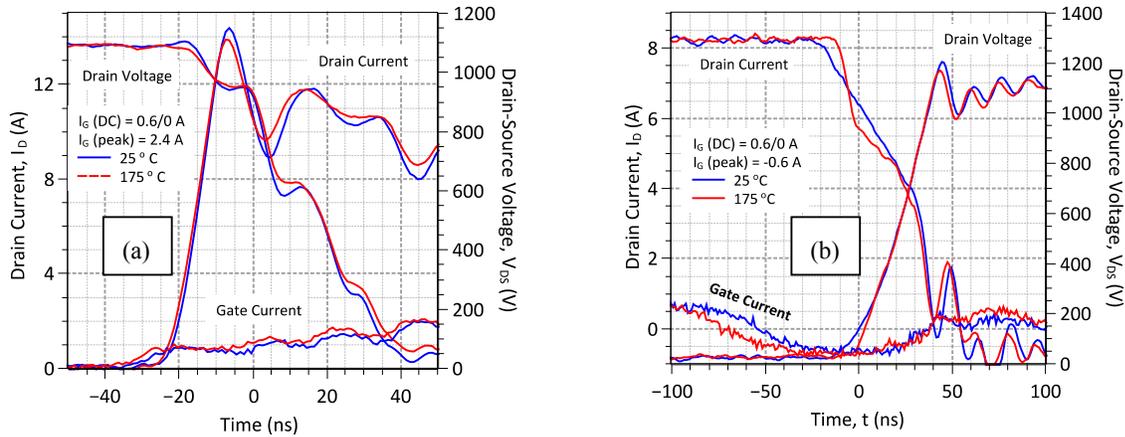


Figure 6 (a) Turn-on and (b) Turn-off waveforms recorded for switching 1100 V and 8 A through a 3.5 mm² SiC SJT. There is no difference in switching speed between 25°C and 250°C, due to the unipolar nature of the SJT device design.

Current Gain Stability

Significant current gain (β) degradation is typically observed when SiC current-controlled transistors (SJT or BJT) are subjected to long-term high-current operation, which remains a key unresolved reliability issue. SiC BJTs or SJTs fabricated even on basal plane dislocation (BPD)-free material are not immune from β degradation, which is attributed to charge trapping by recombination centers in the p-type base layer close to the SiC surface. 1200 V/3.5 mm² SiC SJTs fabricated by the Gen-I process displayed a 25% compression of the current gain [5], when subjected to a 6-hour stress with DC drain current of 200 A/cm², gate current of 0.5 A, and a basplate temperature of 125°C. In stark contrast, 1200 V/3.5 mm² SJTs fabricated by the Gen-II, high-gain process show within 10% β stability even after stressing at base-plate temperatures as high as 145°C (see Fig. 7), which implies a drastic reduction in the the number of recombination centers, which was also inferred from the minimal emitter-size effect shown in Fig. 3.

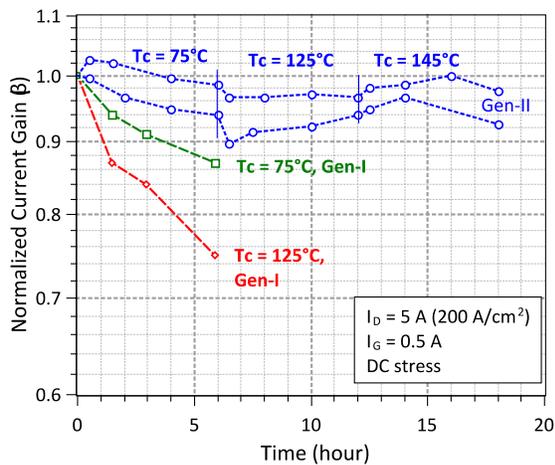


Figure 7: Current Gain degradation of several Gen-I and Gen-II, 1200 V/3.5 mm² SiC SJTs under a 5 A (DC) drain current and 0.5 A gate current stress at various baseplate temperatures. The current gain of the Gen-II SJT is stable within 10% of its pre-test value after 18 hours of cumulative DC current stress at successively increasing base-plate temperatures from 75°C up to 145°C.

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