

Application Note AN-10B: Driving SiC Junction Transistors (SJT): Two-Level Gate Drive Concept

Introduction

GeneSiC Semiconductor is commercializing 1200 V and 1700 V SiC Junction Transistors (SJTs) with current ratings ranging from 3 A to 50 A. SiC SJTs are normally-off, high-performance SiC switches, which are plug-in replacements for Si IGBTs [1-2].

This document is part of a series of application notes which describe optimal gate drive techniques for SiC SJTs. AN-10A describes a simplified gate drive technique, featuring a single commercial IGBT gate driver IC, showing fast switching with low losses. In this document, a more advanced, two voltage level gate drive scheme is described. This technique maintains optimal device switching performance while decreasing the gate drive losses.

Two-Level SJT Gate Drive Circuit

A circuit schematic for the two output voltage level gate drive circuit is shown in Figure 1. It features two commercial gate driver ICs with isolated input signals to protect the gate control signal generator [3]. The gate driver resistor (R_{GP}) and capacitor (C_{GP}) provide improved switching performance, similar to the single-level driver. C_{GP} provides a high transient current peak to the SJT gate terminal at turn-on and turn-off, which charges the base capacitance faster than a constant gate current. C_{GP} is placed in series with resistor R_{Cg} to damp oscillations in this branch. Resistor R_{GP} regulates the steady state gate current after the completion of the transient current peak, dictated by C_{GP} , to maintain the SJT in the on-state. A Si Schottky diode is placed in series with R_{GP} to limit

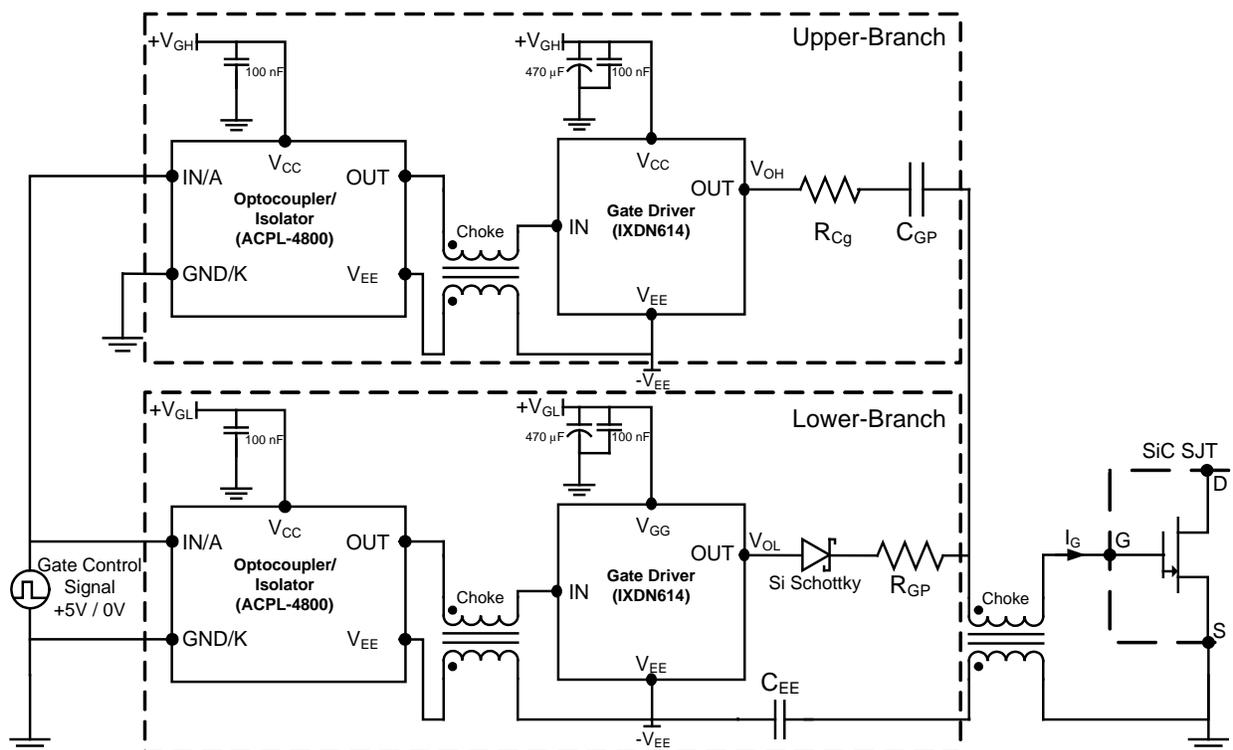


Figure 1: Two-Level SJT Gate Drive Circuit

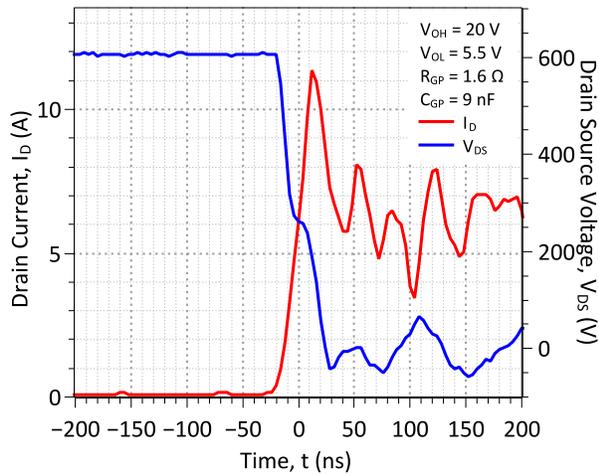


Figure 2: Drain current and voltage waveforms of a 1200 V / 6 A SiC SJT turning on to an inductive load, using a two-level gate driver with suggested parameter values.

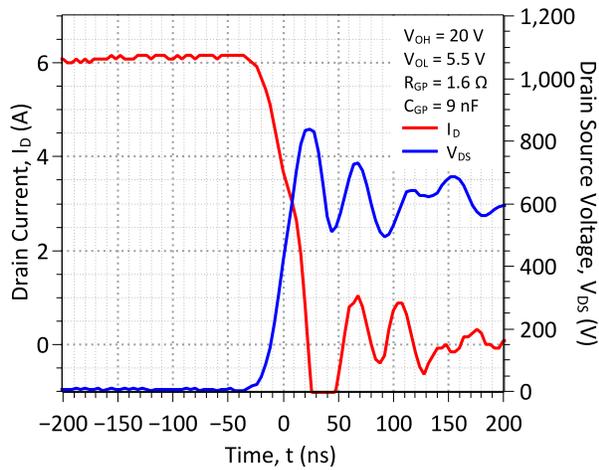


Figure 3: Drain current and voltage waveforms of a 1200 V / 6 A SiC SJT during turn-off, using a two-level gate driver with suggested parameter values.

the transient current from C_{GP} from being drained through the lower-branch of the driver instead of into the SJT gate during the turn-on transient. The selection of these component values is addressed in AN-10A and later in this document.

In the two-level driver, the two gate drive ICs are powered at different voltages, V_{GH} and V_{HL} , allowing for a reduction in driver losses. C_{GP} is driven by the high voltage output V_{OH} in the upper-branch to charge C_{GP} with a high voltage for high

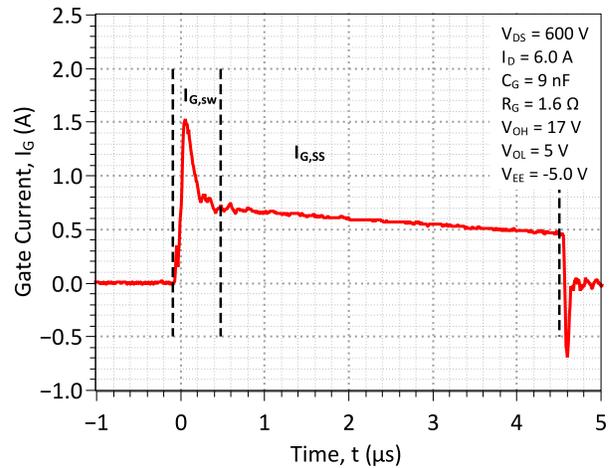


Figure 4: Gate current waveform showing initial transient and steady state time periods while driving a 1200 V / 6 A SJT.

transient gate currents resulting in rapid charging of the SJT's terminal capacitances. R_{GP} is driven by the lower output voltage V_{OL} , which allows for a reduced R_{GP} value compared to the single voltage level driver. Thus the steady state part of the gate drive losses – the largest component of drive loss, is lowered significantly. A representative gate current waveform output from the two-level driver is shown in Figure 4. An initial peak gate current, $I_{G,SW}$ is followed by a steady-state $I_{G,SS}$ around 500 mA.

The low voltage supply, V_{EE} can also be pulled to a negative value for improved switching performance with the inclusion of a coupling capacitor C_{EE} to separate V_{EE} from the grounded SJT source. $C_{EE} \approx 10 \mu\text{F}$ has shown to be an effective value for $V_{EE} = -5 \text{ V}$.

The two-level driver is capable of effectively driving a 1200 V / 6 A SJT as shown in the turn-on and turn-off waveforms of Figure 2 and Figure 3.

Two-Level Driver Parameter Selection

The tradeoffs of adjusting the gate driver passive component values, C_{GP} and R_{GP} in the two-level driver are similar to those described in App Note AN-10A. However the introduction of a

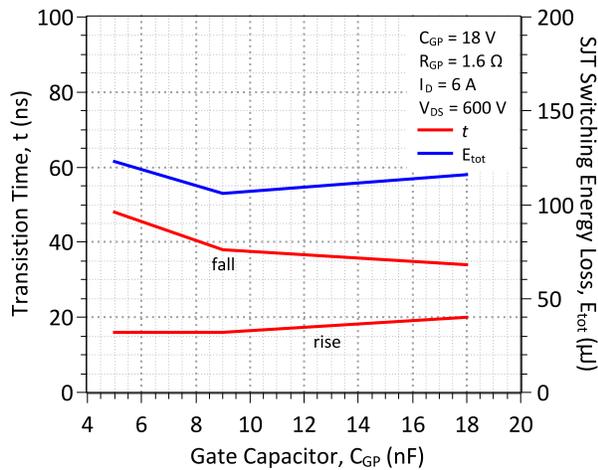


Figure 5: Effect of gate driver capacitance C_{GP} on SJT device current turn-on t_r and turn-off t_f times and total device energy loss.

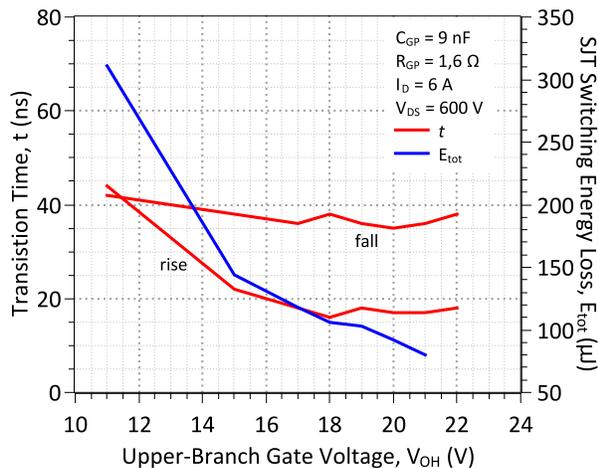


Figure 6: Effect of gate voltage output V_{OH} on SJT current transition times and total device switching energy loss.

second gate voltage affects the optimal parameter values which obtain the best driver and device switching performance.

During device turn-on, the dynamic gate current transient ($I_{G,SW}$ in the Figure 4 gate current waveform) is determined by V_{OH} and C_{GP} , which dominates the transient behavior of the device, similar to the single-level driver circuit. However in the two-level scheme, the gate current through the high output voltage branch goes to zero, once C_{GP} is fully charged.

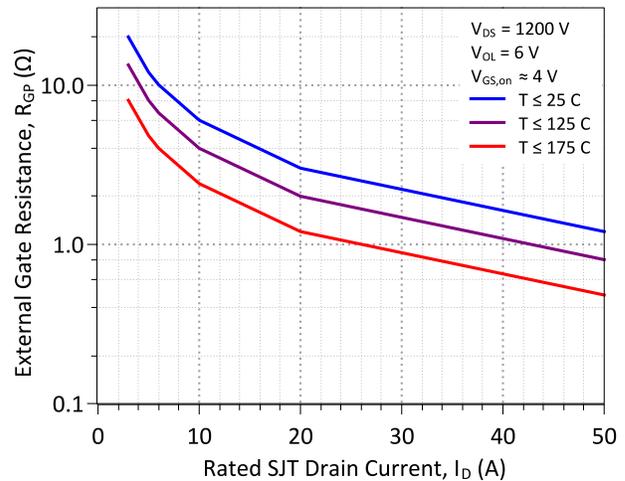


Figure 7: Suggested R_{GP} values for 1200 V, GAXXJTX series SJTs for $V_{OL} = 6.0$ V.

It is shown in Figure 5 for a 1200 V / 6 A SJT that at $C_{GP} = 9$ nF, the SJT drain current switching times, t_r , t_f and device switching energy losses, E_{tot} are at their combined lowest values.

It is shown in Figure 6 that device current transition times and energy losses are lowest at $V_{OH} = 20$ V. The upper-branch series resistor R_{CG} acts solely to damp oscillations in the circuit path of C_{GP} and should be valued around 1 Ω and have low inductance.

During steady on-state operation, after device turn-on (see Figure 4), the gate current $I_{G,ss}$ is determined by the lower branch voltage, V_{OL} and output resistor, R_{GP} . Current will begin passing through R_{GP} once the gate voltage on the device introduced by C_{GP} drops below V_{OL} . V_{OL} must exceed the SJT on-state gate-source voltage V_{GS} while the SJT is conducting drain current. For typical condition, $V_{GS} \approx 4.0$ V, thus $V_{OL} \geq 5.5$ V is acceptable value to maintain steady gate current and $V_{OL} = 5.5$ V has been used for all testing in this paper in combination with $R_{GP} = 1.6\Omega$. These conditions supply ~ 500 mA of gate current even with minor transient fluctuation of $V_{GS,on}$ and maintain the SJT in the saturation region, even at 175 $^{\circ}\text{C}$. This gate current is higher than what is required to turn the device on, however it is

Table 1: Optimal Gate Drive Parameter Values

Parameter	Single-Level	Two-Level
V_{OH}	15 V	20 V
V_{OL}	15 V	6.0 – 5.5 V
V_{EE}	GND	- 5.0 V
C_{GP}	9 nF	9 nF
R_{GP}	22 Ω	1.6 Ω

Table 2: Gate Drive Power Loss Comparison Example

$D = 0.7, f_0 = 500 \text{ kHz}, V_{DS} = 600 \text{ V}, I_D = 6 \text{ A}$		
Parameter	Single-Level	Two-Level
$P_{drive,ss}$	3.85 W	0.45 W
$P_{drive,sw}$	0.54 W	1.15 W
$P_{SJT,sw}$	45.6 W	46.0 W
Total	54.7 W	52.28 W

suggested to overdrive an SJT in most applications to ensure operation at a low V_{DS} value. At higher temperatures more gate current is required to operate an SJT with V_{DS} in the lowest possible range and thus lower gate resistances are required for this higher gate current to flow into the device for a fixed V_{OL} . Suggested R_{GP} values are shown in Figure 7 for certain devices.

Gate Drive Power Loss Comparison

Power loss occurs in both the transistor and the gate drive circuitry and is a function of the gate drive circuit, parameter values, switching frequency f_0 , and duty cycle D . The gate drive losses are comprised of the steady-state resistive loss, $P_{drive,SS}$ and capacitive switching loss, $P_{drive,Sw}$. Among the several SJT power losses, switching loss $P_{SJT,Sw}$ is extremely sensitive to the specific gate drive configuration. These losses can be calculated as:

$$P_{drive,ss} = (V_{OL} - V_{GSon})(D - t_s f_0)I_{g,ss},$$

$$P_{drive,sw} = C_{GP}(V_{GH} - V_{GSon})^2 f_0$$

and

$$P_{SJT,sw} = E_{tot} f_0,$$

where t_s is the turn-on transient time shown in Figure 4 and E_{tot} is the total SJT switching energy lost in one switch cycle [4]. From these driver dependant losses, it can be determined which gate drive topology, single or two-level, yields the lowest total power loss for a particular system operating frequency and duty cycle.

There is a power loss component arising from the gate current flowing through the SJT gate-source junction, P_{GS} , as well as the power loss associated with charging the gate capacitance, P_{GC} . These two loss contributors are largely independent of the gate driver topology, and differ by only a few milliwatts between the single and two-level gate drive. Therefore, these losses are not considered in this discussion comparing the gate drive topologies.

An analysis is performed of only the driver dependent losses between the two optimized gate drives when driving a 1200 V / 6 A SJT at 500 kHz with a duty cycle of 0.7. The gate-drive parameter values are shown in Table 1 and the power losses are shown in Table 2 [5]. It can be observed in Table 2 that use of the two-level driver lowers system power loss due to the reduced driver steady state losses $P_{drive,SS}$. Power loss components not shown are not dependant on the gate drive topology. Lower steady state losses in the two level driver translates to even greater power savings for increased duty cycles, as shown in Figure 8.

The device power losses in each switching cycle (which constitute the largest fraction of all

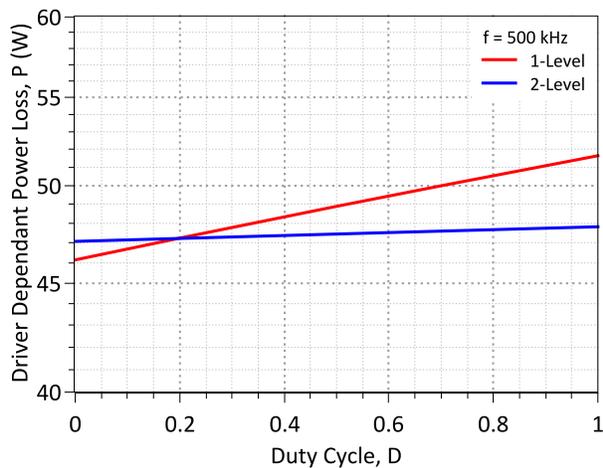


Figure 8: System power loss versus duty cycle for a fixed switching frequency f .

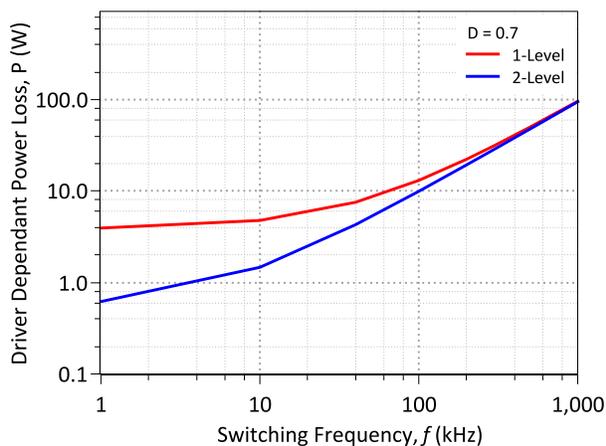


Figure 9: System power loss versus frequency analysis for a fixed duty cycle D .

loss components) are very similar for both drivers. Therefore, there is a weak dependence of the difference in power loss between the two drivers on switching frequency. Thus for a constant duty cycle, the two-level driver will have an approximately constant power savings compared to the single-level driver for frequencies below ~ 500 kHz. The two-level driver will continue to have lower total power loss at frequencies below 1.7 MHz for $D \geq 0.5$. This constant power savings value for the two-level driver is shown in Figure 9 for $f < 1.0$ MHz and $D = 0.7$. Thus, the two-level

driver offers a lower total power loss in nearly any SJT application.

Summary

SiC Junction Transistors are capable of fast switching speeds with ultra-low losses without the drawbacks of other SiC transistors or Si IGBTs. A gate drive schematic is presented in this application for lowering the overall system power loss due to a reduction of steady state gate driver losses compared to the simpler single-level driver presented in AN-10A. Considerations of passive component value selection are discussed and the benefits and drawbacks of each approach are explained.

References

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